Features
- Compact packaging supports slimmer set designs
- Series designed from 50 up to 150 W and pin-compatibility
- Simpler heat sink design facilitates thermal design of slim stereo sets
- Current mirror circuit, cascade circuit and pure-complimentary circuit apply reduce distortion to 0.008 %
- Supports addition of electronic circuits for thermal shutdown and load-short protection circuit as well as pop noise muting which occurs when the power supply switch is turned on and off.

Specifications
Maximum Ratings at Ta = 25°C

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Ratings</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum supply voltage</td>
<td>VCC max</td>
<td></td>
<td>± 74 V</td>
<td>V</td>
</tr>
<tr>
<td>Thermal resistance</td>
<td>θjc</td>
<td></td>
<td>1.2 °C/W</td>
<td>°C/W</td>
</tr>
<tr>
<td>Junction temperature</td>
<td>TJ</td>
<td></td>
<td>150 °C</td>
<td>°C</td>
</tr>
<tr>
<td>Operating substrate temperature</td>
<td>TC</td>
<td></td>
<td>125 °C</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>Tstg</td>
<td></td>
<td>-30 to +125 °C</td>
<td>°C</td>
</tr>
<tr>
<td>Permissible load short time</td>
<td>tbc</td>
<td>VCC = ± 51 V, RL = 8 Ω, f = 50 Hz, PO = 100 W</td>
<td>1 s</td>
<td></td>
</tr>
</tbody>
</table>

Recommended Operating Conditions at Ta = 25°C

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Ratings</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Recommended supply voltage</td>
<td>VCC</td>
<td></td>
<td>± 51 V</td>
<td>V</td>
</tr>
<tr>
<td>Load resistance</td>
<td>RL</td>
<td></td>
<td>8 Ω</td>
<td></td>
</tr>
</tbody>
</table>

Operating Characteristics
at Ta = 25°C, VCC = ± 51 V, RL = 8 Ω, VG = 40 dB, Rg = 600 Ω, 100 kHz LPF ON, RL (noninductive)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Ratings</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Quiescent current</td>
<td>ICCO</td>
<td>VCC = ± 61.5 V</td>
<td>15</td>
<td>mA</td>
</tr>
<tr>
<td>Output power</td>
<td>PO</td>
<td>THD = 0.008 %, I = 20 Hz to 20 kHz</td>
<td>100</td>
<td>W</td>
</tr>
<tr>
<td>Total harmonic distortion</td>
<td>THD</td>
<td>PO = 1.0 W, I = 1 kHz</td>
<td>0.008 %</td>
<td>%</td>
</tr>
<tr>
<td>Frequency response</td>
<td>f1, f3</td>
<td>PO = 1.0 W, f = 1 kHz</td>
<td>20 to 50k Hz</td>
<td>Hz</td>
</tr>
<tr>
<td>Input resistance</td>
<td>Ri</td>
<td>PO = 1.0 W, f = 1 kHz</td>
<td>55</td>
<td>kΩ</td>
</tr>
<tr>
<td>Output noise voltage</td>
<td>VNO2</td>
<td>VCC = ± 61.5 V, Rg = 10 kΩ</td>
<td>1.2</td>
<td>mVrms</td>
</tr>
<tr>
<td>Neutral voltage</td>
<td>VN</td>
<td>VCC = ± 61.5 V</td>
<td>-70</td>
<td>mV</td>
</tr>
</tbody>
</table>

Note: Use rated power supply for test unless otherwise specified.

# SANYO Electric Co., Ltd. Semiconductor Business Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN
Specified Transformer Power Supply
(MG-200 Equivalent)

Equivalent Circuit

Sample Application Circuit: 100W min Single Channel AF Power Amplifier
Sample Printed Circuit Pattern for Application Circuit (Copper-foiled side)

Description of External Parts

R₁, C₁ : Input filter circuit
- Reduces high-frequency noise.

C₂ : Input coupling capacitor
- DC current suppression. A reduction in reactance is effective because of increases in capacitor reactance at low frequencies and 1/f noise dependence on signal source resistance which result in output noise worsening.

R₂ : Input bias resistor
- Biases the input pin to zero.
- Effects Vᵦ stability (refer to NF circuit).
- Due to differential input, input resistance is more or less determined by this resistance value.

R₄, R₅ : NFB circuit (AC NF circuit). Use of resistor with 1% error is suggested.

C₃ (R₃) : AC NF capacitor

R₄, R₅ : Used for VG setting.
• VG settings are obtained using $R_4$ and $R_5$ according to the following equation:

$$\log_{20} \frac{R_5}{R_4} \quad 40 \text{ dB is recommended.}$$

• Low-frequency cutoff frequency settings are obtained using $R_4$ and $C_3$ according to the following equation:

$$f_L = \frac{1}{2\pi R_4 C_3} \quad [\text{Hz}]$$

When changing the VG setting, you should change $R_4$ which requires a recheck of the low cutoff frequency setting. When the VG setting is changed using $R_5$, the setting should ensure $R_5$ equals $R_4$ so that $V_N$ balance stability is maintained. If the resistor value is increased more than the existing value, $V_N$ balance may be disturbed and result in deterioration of $V_N$ temperature characteristics.

$R_3$ : Differential constant-current bias resistor

$R_6, R_7$ : For oscillation suppression and phase compensation applications
(For use with differential stage applications)

$R_7, C_4$ : For oscillation suppression and phase compensation applications
(A Mylar capacitor is recommended for $C_4$ for use with output stage applications)

$C_6, C_9$ : For oscillation suppression and phase compensation applications

$C_8$ : Power stage (Must be connected near the pin)  $C_6$: Positive (+) power  $C_9$: Negative (−) power

$C_5$ : For oscillation suppression and phase compensation applications
(For use with differential stage applications)

$R_8, C_{10}$ : For oscillation suppression and distortion improvement applications

$R_9, C_{13}$ : Ripple filter circuit on positive (+) side.

$C_{11}, C_{12}$ : Ripple filter circuit on negative (−) side.

$C_{11}, C_{12}$ : For oscillation suppression applications

• Used for reducing power supply impedance to stable IC operation and should be connected near the IC pin. We recommend that you use an electrolytic capacitor.

$R_{10}$ : Output resistor

Increases load shorting endurance capacity during times of high output.

$R_{14}, L_1$ : For oscillation suppression applications

Increases oscillation stability against capacitance loads.