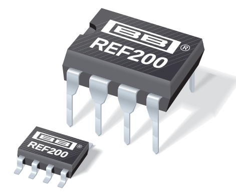
BURR - BROWN®

REF200



DUAL CURRENT SOURCE/CURRENT SINK

FEATURES

- COMPLETELY FLOATING: No Power Supply or Ground Connections
- HIGH ACCURACY: 100µA ±0.5%
- LOW TEMPERATURE COEFFICIENT: ±25ppm/°C
- WIDE VOLTAGE COMPLIANCE: 2.5V to 40V
- ALSO INCLUDES CURRENT MIRROR

APPLICATIONS

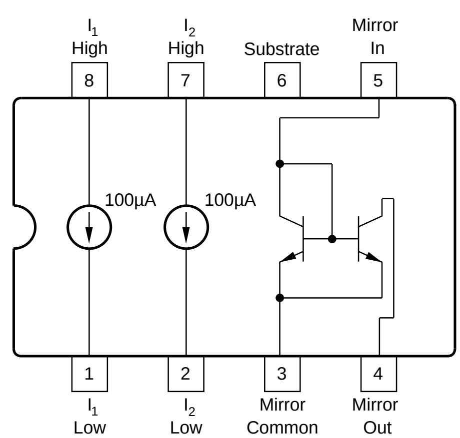
- SENSOR EXCITATION
- BIASING CIRCUITRY
- OFFSETTING CURRENT LOOPS
- LOW VOLTAGE REFERENCES
- CHARGE-PUMP CIRCUITRY
- HYBRID MICROCIRCUITS

DESCRIPTION

The REF200 combines three circuit building-blocks on a single monolithic chip—two 100µA current sources and a current mirror. The sections are dielectrically isolated, making them completely independent. Also, since the current sources are two-terminal devices, they can be used equally well as current sinks. The performance of each section is individually measured and laser-trimmed to achieve high accuracy at low cost.

The sections can be pin-strapped for currents of 50µA, 100µA, 200µA, 300µA or 400µA. External circuitry can be used to obtain virtually any current. These and many other circuit techniques are shown in the Applications section of this Data Sheet.

The REF200 is available in plastic 8-pin mini-DIP and SOIC packages.



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PDS-851D

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SBVS020

SPECIFICATIONS

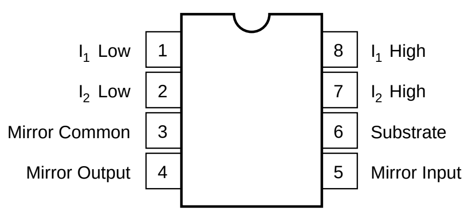
ELECTRICAL

At T_A = +25°C, V_S = 15V, unless otherwise noted.

PARAMETER	CONDITION	REF200AP, AU MIN	TYP	MAX	UNITS
CURRENT SOURCES					
Current Accuracy			±0.25	±1	%
Current Match			±0.25	±1	%
Temperature Drift	Specified Temp Range		25		ppm/°C
Output Impedance	2.5V to 40V	20	100		MΩ
	3.5V to 30V	200	500		MΩ
Noise	BW = 0.1Hz to 10Hz		1		nAp-p
	f = 10kHz		20		pA/$\sqrt{Hz}$
Voltage Compliance (1%)	T_{MIN} to T_{MAX}		See Curves		
Capacitance			10		pF
CURRENT MIRROR	I = 100µA Unless Otherwise Noted				
Gain		0.995	1	1.005	
Temperature Drift			25		ppm/°C
Impedance (output)	2V to 40V	40	100		MΩ
Nonlinearity	I = 0µA to 250µA		0.05		%
Input Voltage			1.4		V
Output Compliance Voltage			See Curves		
Frequency Response (–3dB)	Transfer		5		MHz
TEMPERATURE RANGE					
Specification		–25		+85	°C
Operating		–40		+85	°C
Storage		–40		+125	°C

PIN CONFIGURATION

Top View **DIP/SOIC**



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

Applied Voltage	–6V to +40V
Reverse Current	–350µA
Voltage Between Any Two Sections	±80V
Operating Temperature	–40°C to +85°C
Storage Temperature	–40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
(SOIC 3s)	+260°C

PACKAGE/ORDERING INFORMATION

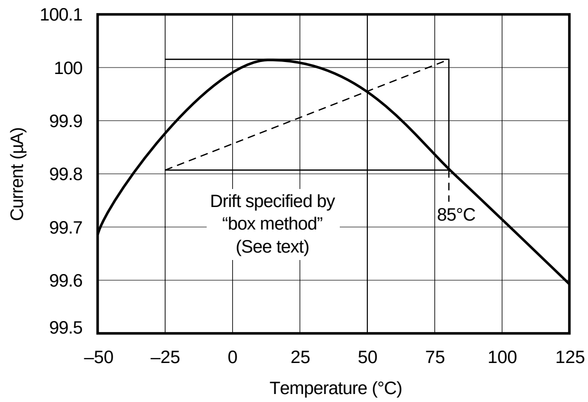
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)	TEMPERATURE RANGE
REF200AP	8-Pin Plastic DIP	006	–25°C to +85°C
REF200AU	8-Pin SOIC	182	–25°C to +85°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Grade designation "A" may not be marked. Absence of grade designation indicates A grade.

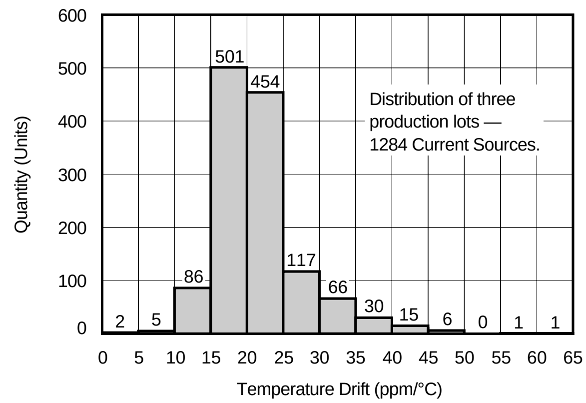
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_S = +15V, unless otherwise noted.

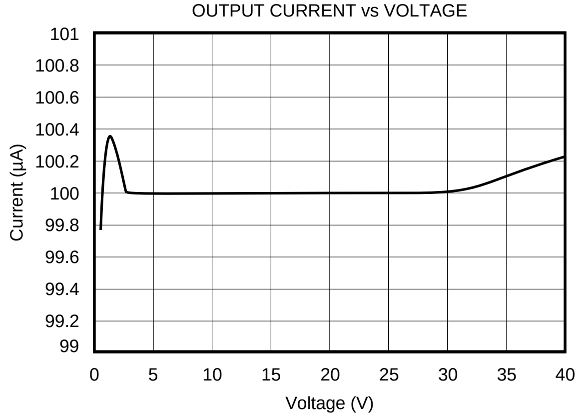
CURRENT SOURCE
TYPICAL DRIFT vs TEMPERATURE



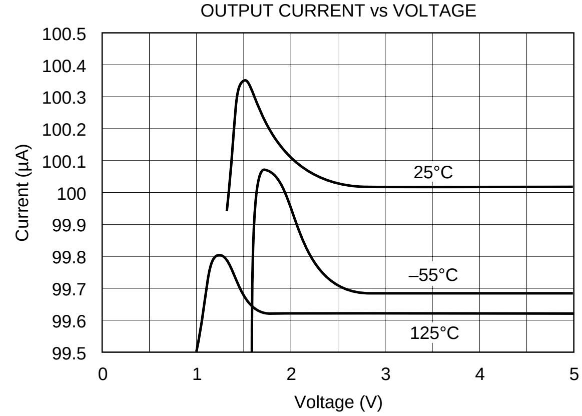
CURRENT SOURCE
TEMPERATURE DRIFT DISTRIBUTION



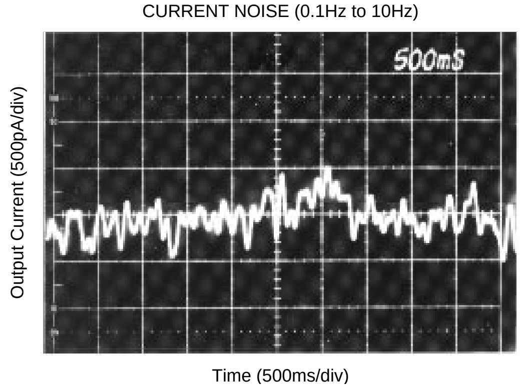
CURRENT SOURCE
OUTPUT CURRENT vs VOLTAGE



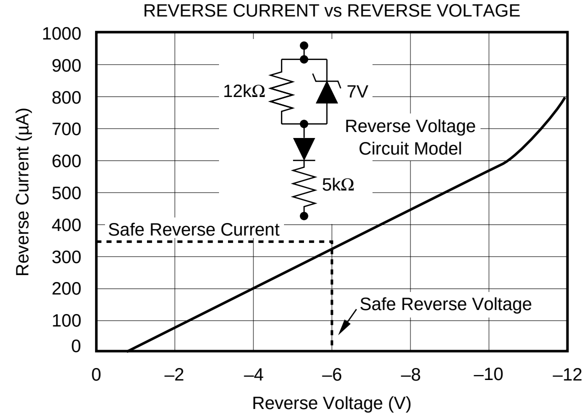
CURRENT SOURCE
OUTPUT CURRENT vs VOLTAGE



CURRENT SOURCE
CURRENT NOISE (0.1Hz to 10Hz)

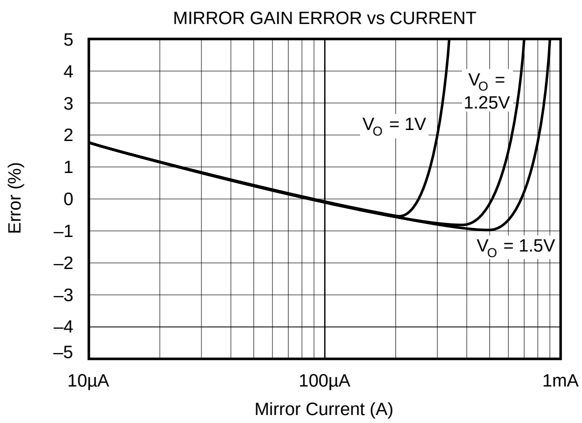


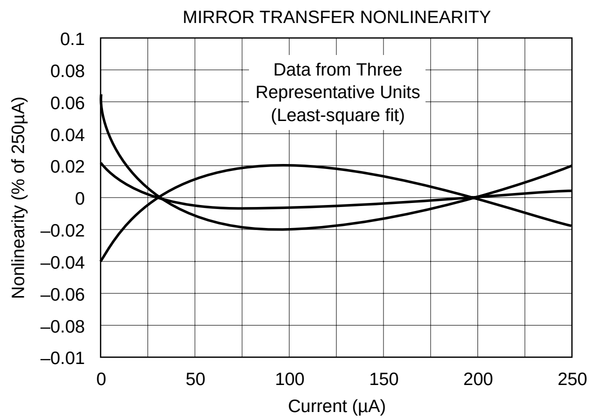
CURRENT SOURCE
REVERSE CURRENT vs REVERSE VOLTAGE

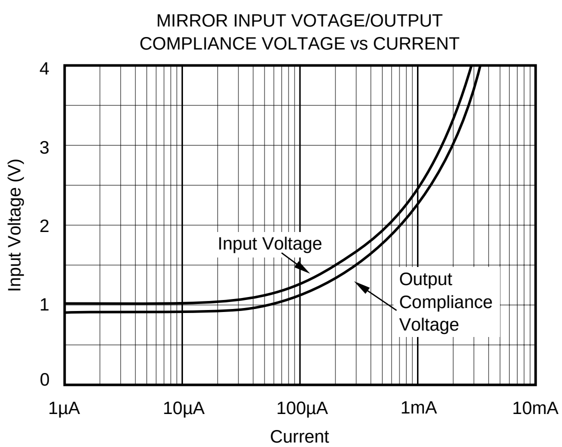


TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = +15V, unless otherwise noted.







APPLICATIONS INFORMATION

The three circuit sections of the REF200 are electrically isolated from one another using a dielectrically isolated fabrication process. A substrate connection is provided (pin 6), which is isolated from all circuitry. This pin should be connected to a defined circuit potential to assure rated DC performance. The preferred connection is to the most negative constant potential in your system. In most analog systems this would be $-V_S$. For best AC performance, leave pin 6 open and leave unused sections unconnected.

Drift performance is specified by the "box method," as illustrated in the Current vs Temperature plot of the typical performance curves. The upper and lower current extremes measured over temperature define the top and bottom of the box. The sides are determined by the specified temperature range of the device. The drift of the unit is the slope of the diagonal—typically 25ppm/°C from –25°C to +85°C.

If the current sources are subjected to reverse voltage, a protection diode may be required. A reverse voltage circuit model of the REF200 is shown in the Reverse Current vs Reverse Voltage curve. If reverse voltage is limited to less than 6V *or* reverse current is limited to less than 350µA, no protection circuitry is required. A parallel diode (Figure 2a) will protect the device by limiting the reverse voltage across the current source to approximately 0.7V. In some applications, a series diode may be preferable (Figure 2b) because it allows no reverse current. This will, however, reduce the compliance voltage range by one diode drop.

Applications for the REF200 are limitless. Application Bulletin AB-165 shows additional REF200 circuits as well as other related current source techniques. A collection of circuits is shown to illustrate some techniques. Also, see AB-165A.

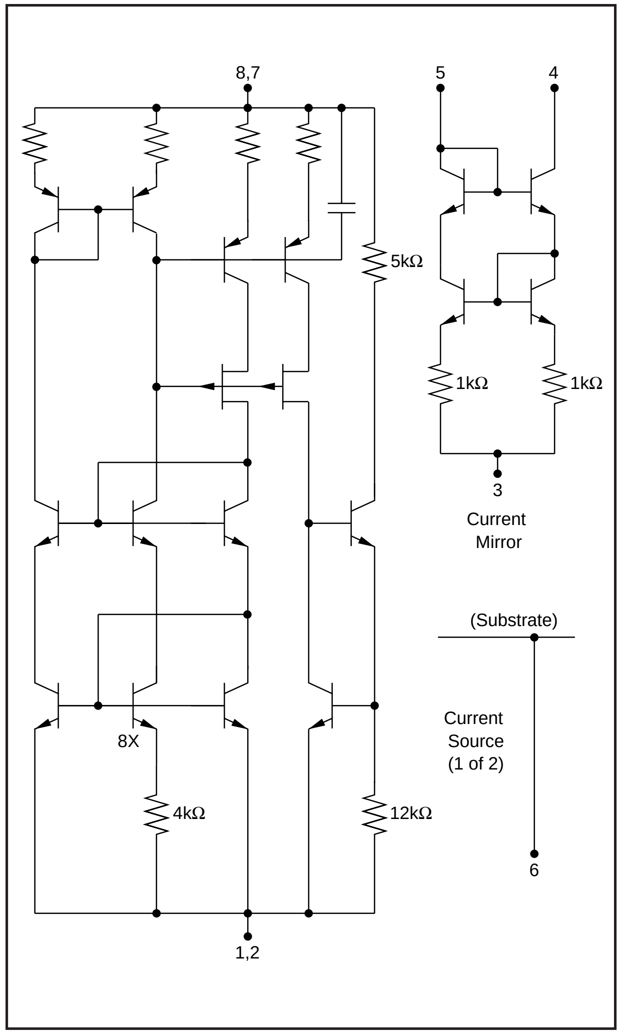


FIGURE 1. Simplified Circuit Diagram.

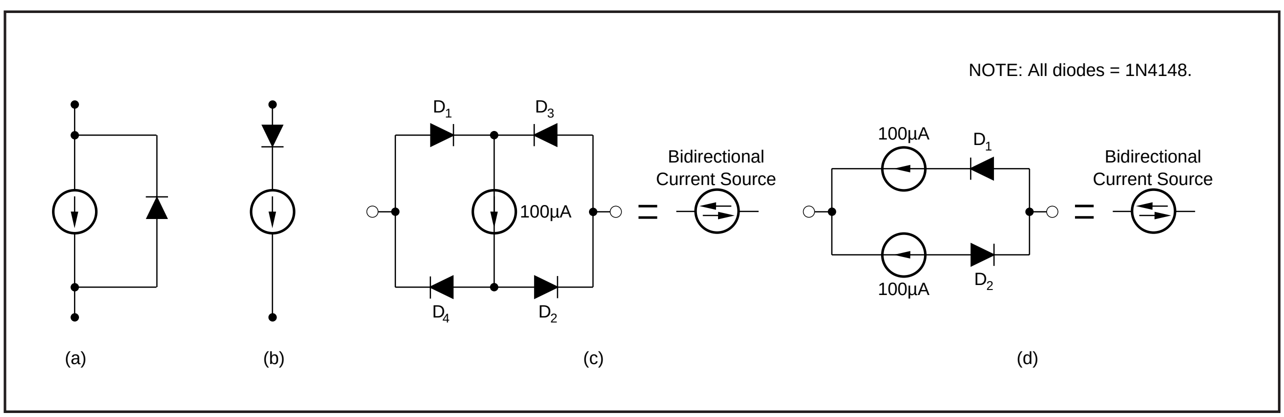


FIGURE 2. Reverse Voltage Protection.

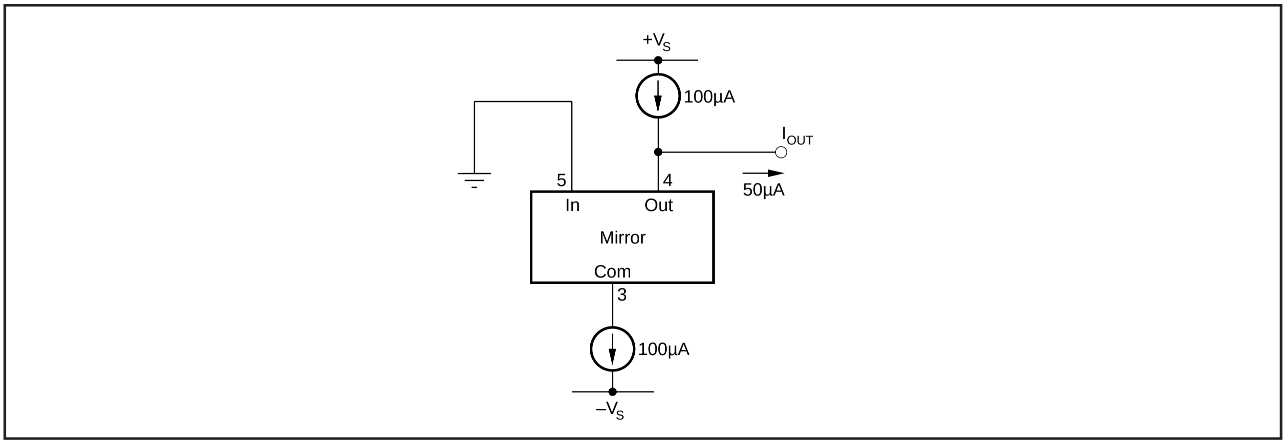


FIGURE 3. 50µA Current Source.

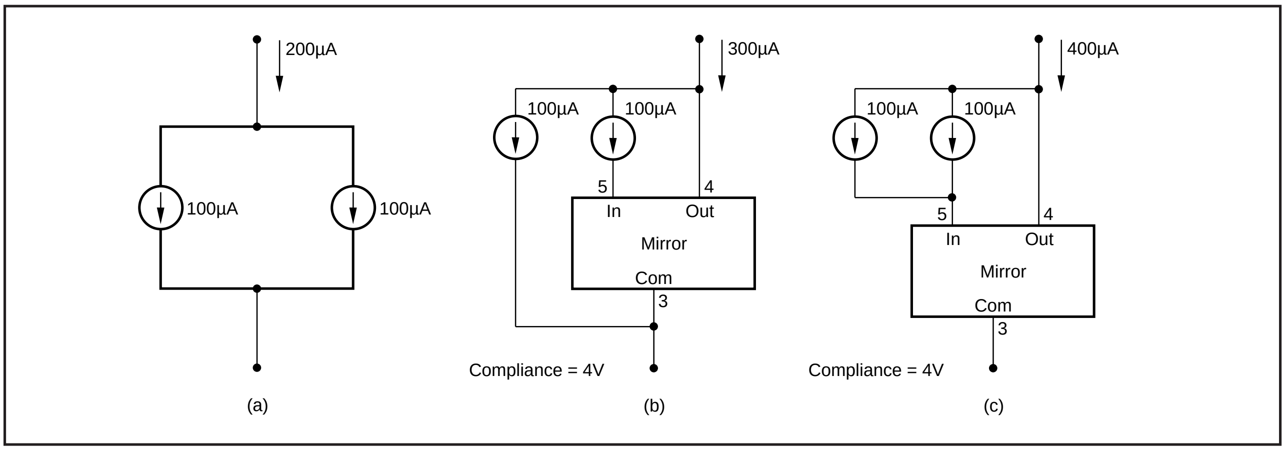


FIGURE 4. 200µA, 300µA, and 400µA Floating Current Sources.

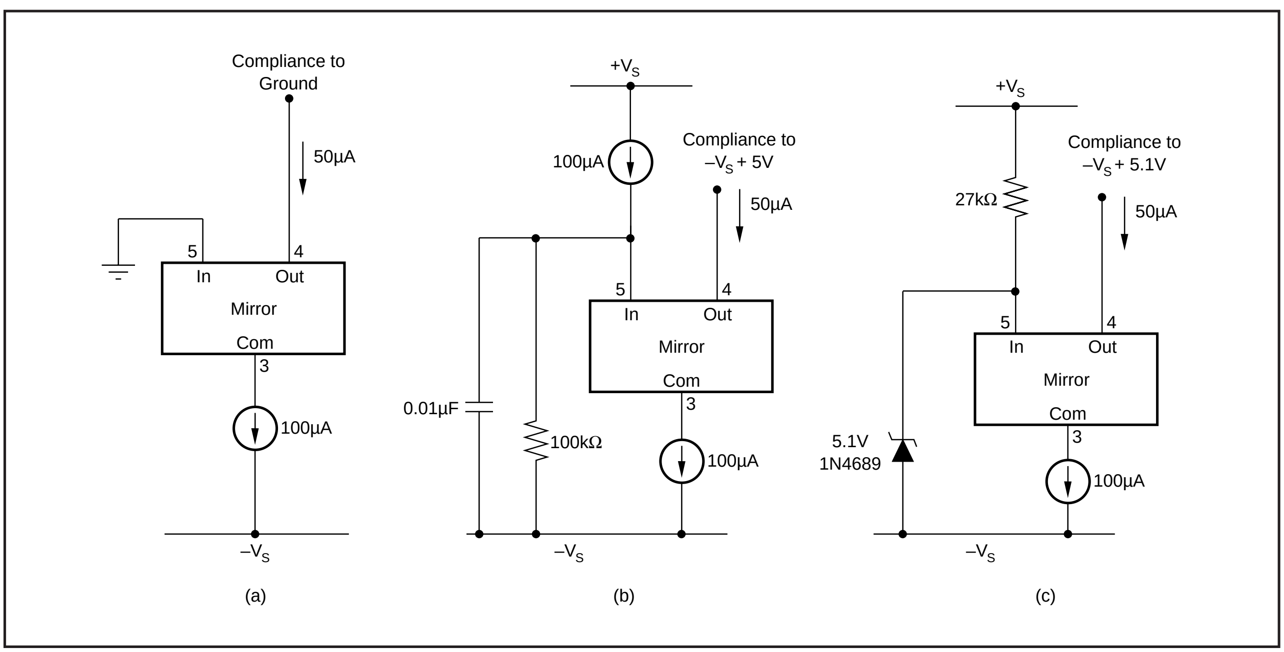


FIGURE 5. 50µA Current Sinks.

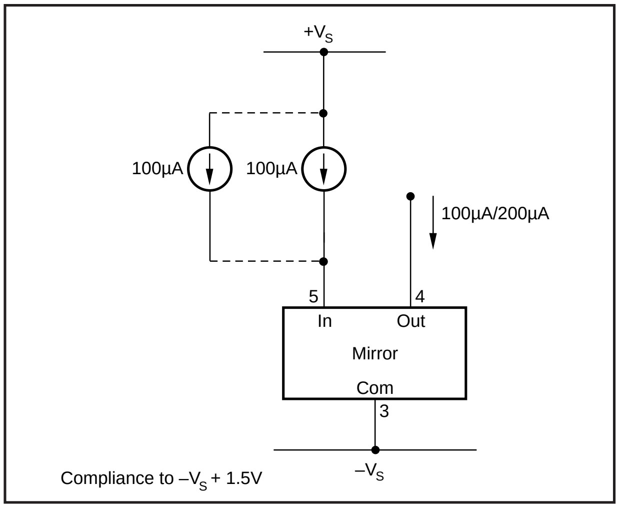


FIGURE 6. Improved Low-Voltage Compliance.

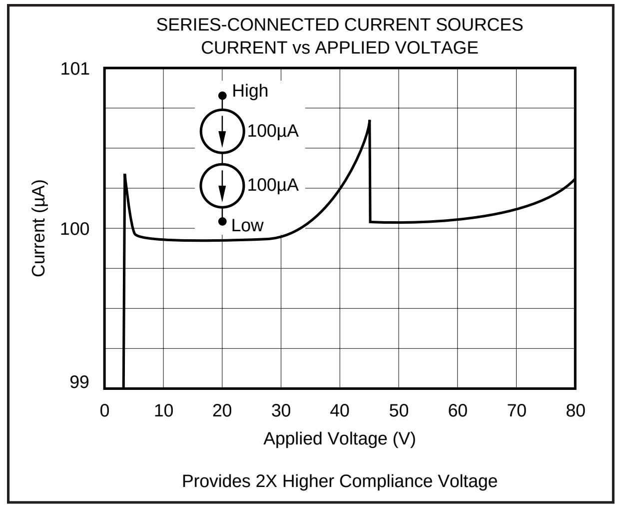


FIGURE 7. 100µA Current Source—80V Compliance.

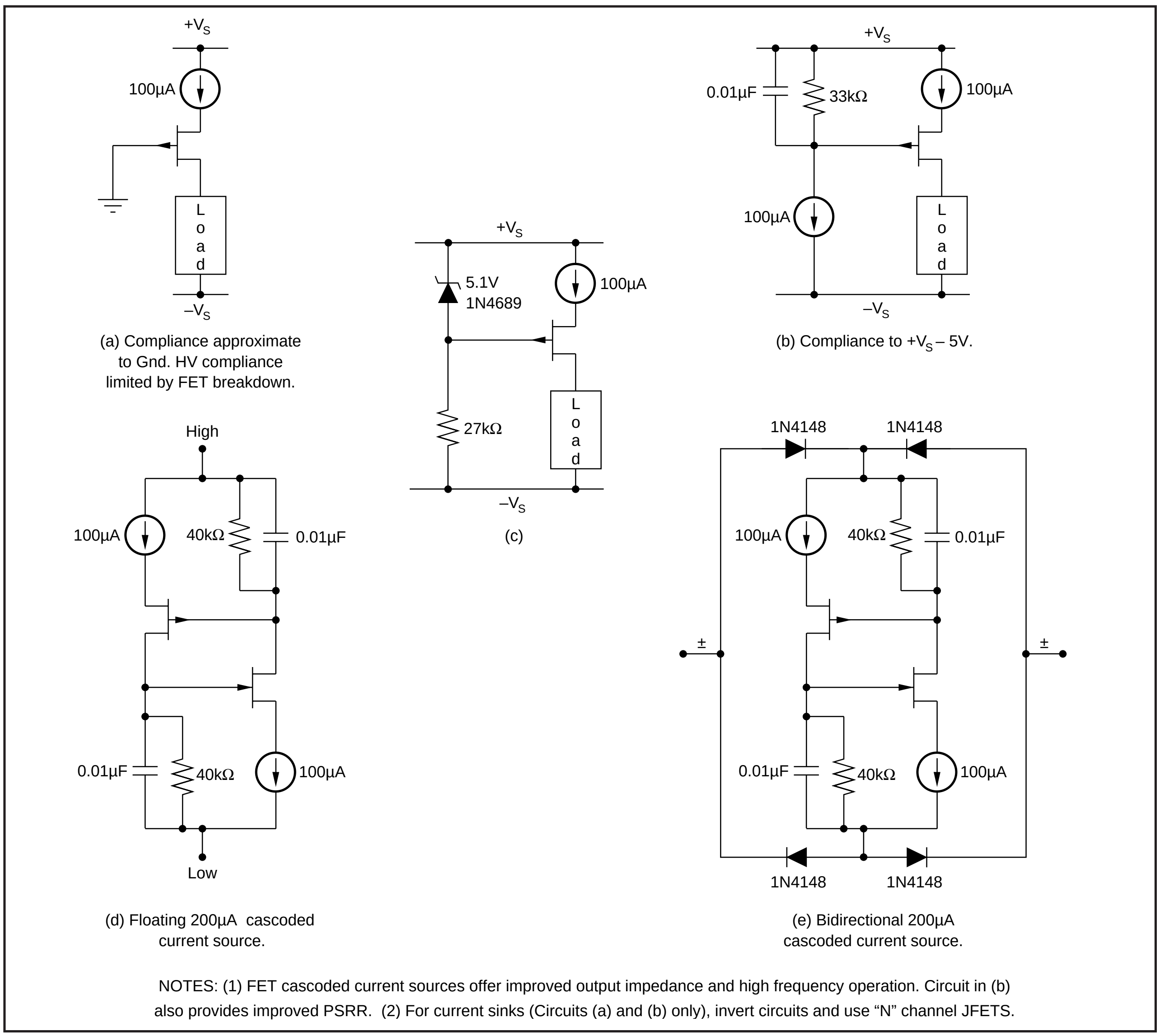


FIGURE 8. FET Cascode Circuits.

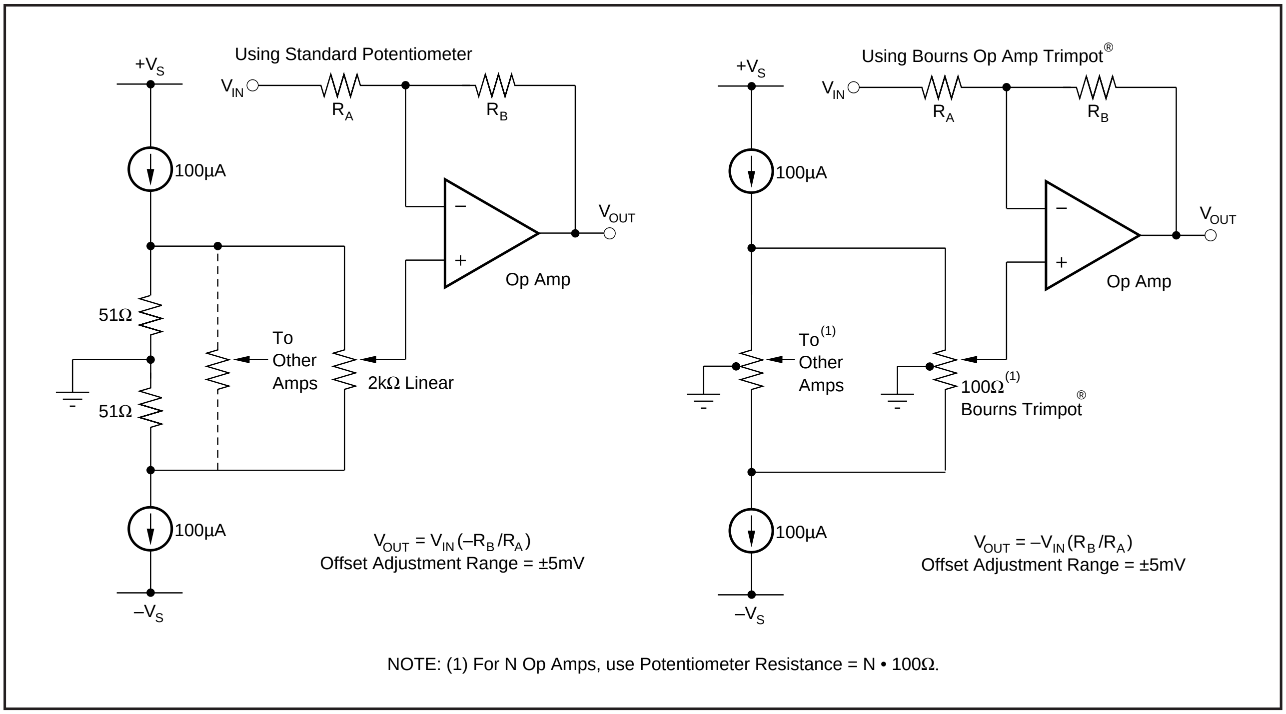
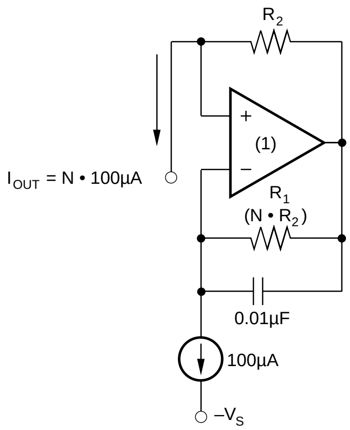


FIGURE 9. Op Amp Offset Adjustment Circuits.



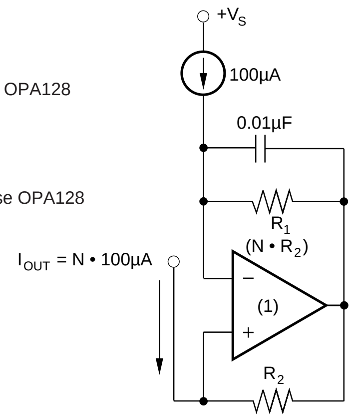
(a)

NOTE: (1) Burr Brown® OPA602 or OPA128

EXAMPLES

R_1	R_2	I_{OUT}
100Ω	10MΩ	1nA
10kΩ	1MΩ	1µA
10kΩ	1kΩ	1mA

→ Use OPA128



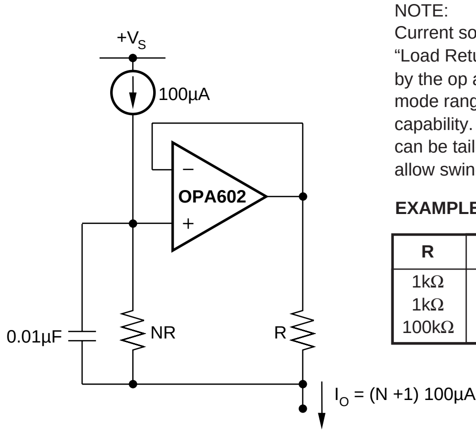
(b)

FEATURES:
(1) Zero volts shunt compliance.
(2) Adjustable only to values above reference value.

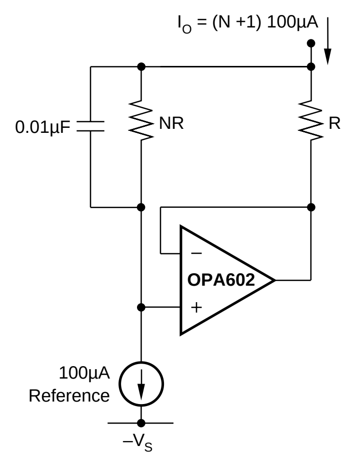
NOTE:
Current source/sink swing to the "Load Return" rail is limited only by the op amp's input common mode range and output swing capability. Voltage drop across "R" can be tailored for any amplifier to allow swing to zero volts from rail.

EXAMPLES

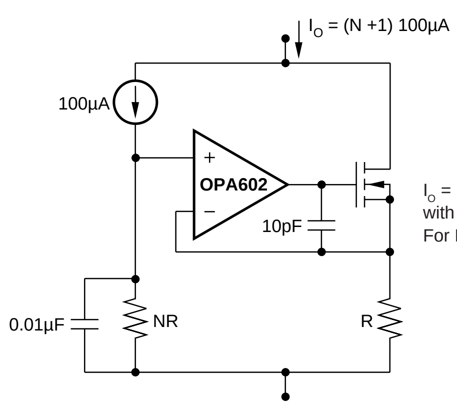
R	NR	I_{OUT}
1kΩ	4kΩ	500µA
1kΩ	9kΩ	1mA
100kΩ	9.9kΩ	10mA



(c)



(d)



I_O = 100µA (N + 1). Compliance ≈ 3.5V with 0.1V across R. Max I_O limited by FET. For I_O = 1A, R = 0.1Ω, NR = 1kΩ.

(e)

FIGURE 10. Adjustable Current Sources.

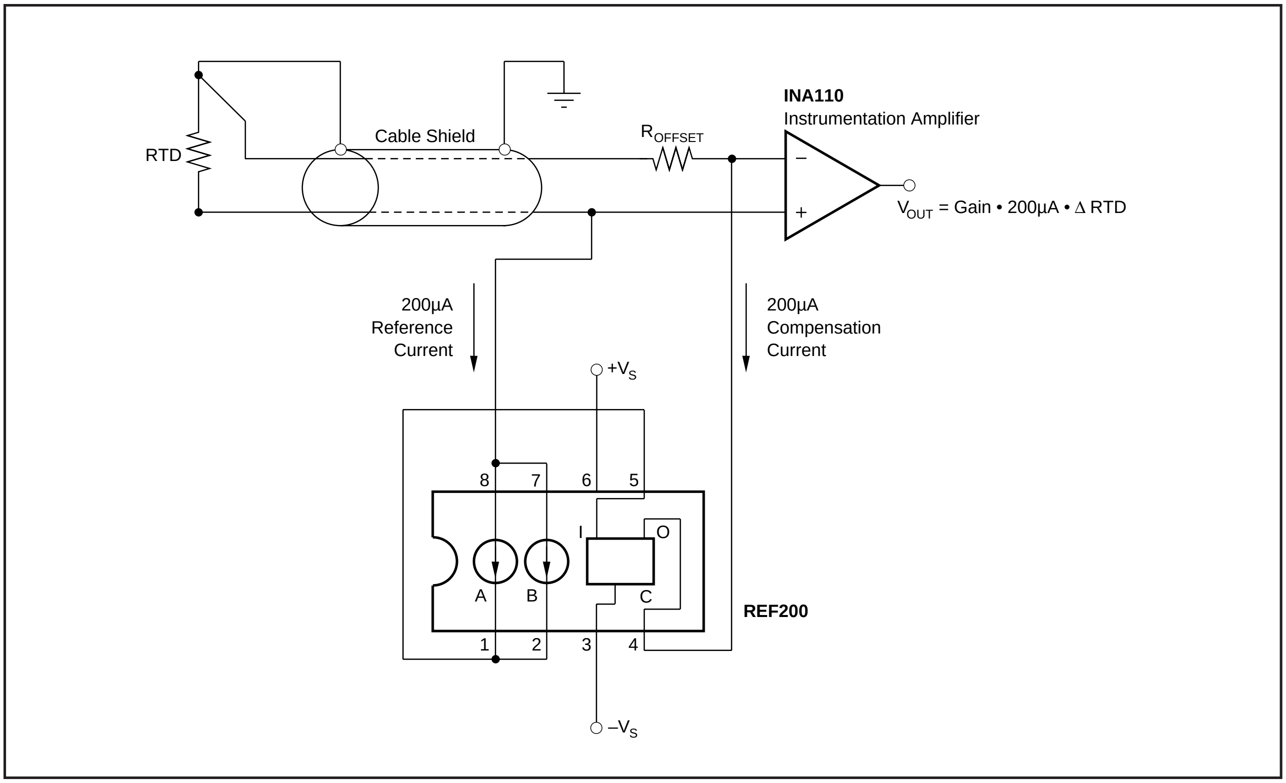


FIGURE 11. RTD Excitation With Three Wire Lead Resistance Compensation.

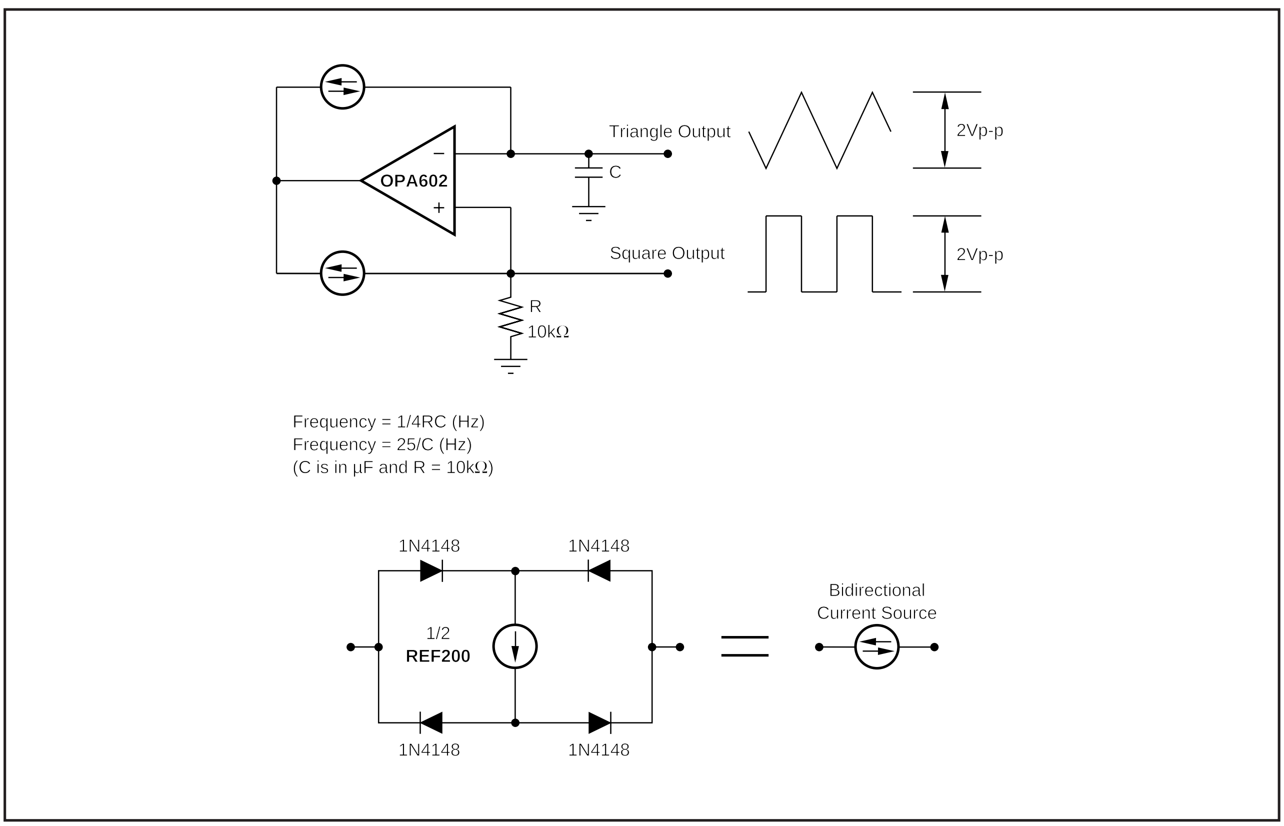


FIGURE 12. Precision Triangle Waveform Generator.

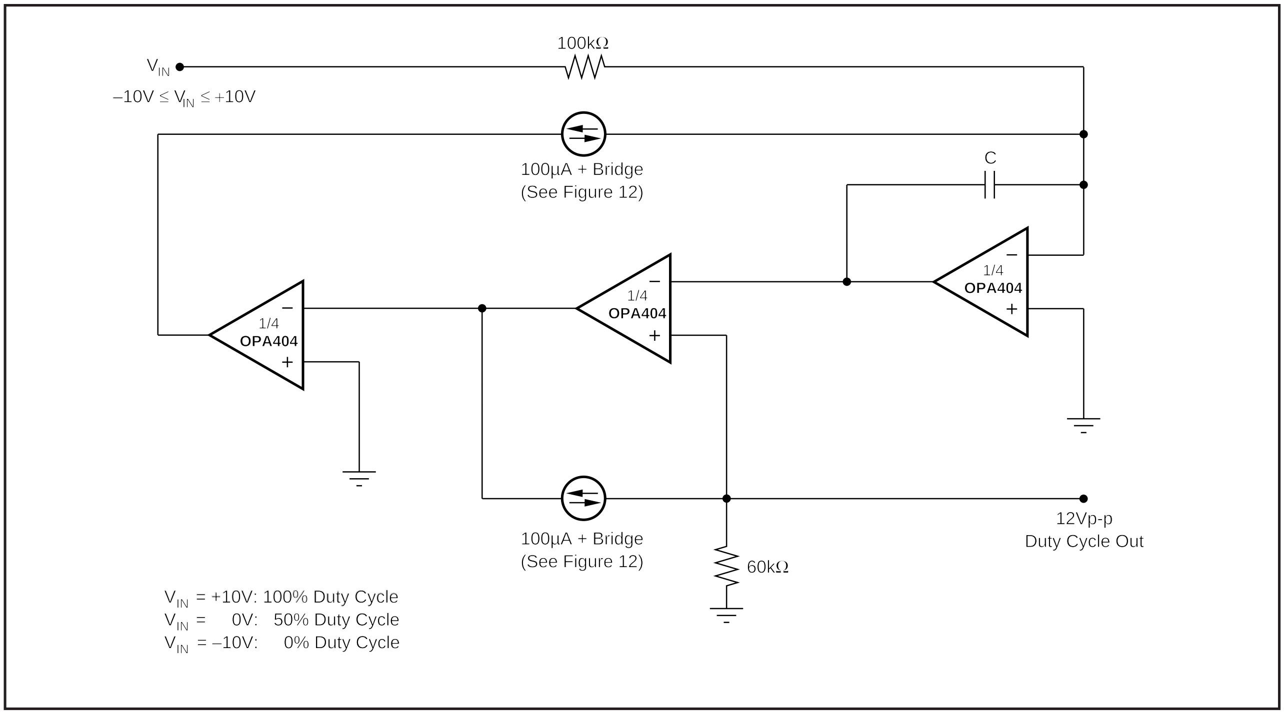


FIGURE 13. Precision Duty-Cycle Modulator.

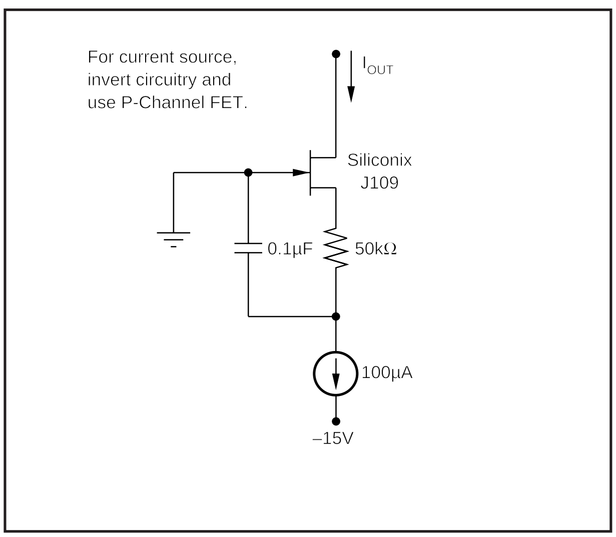


FIGURE 14. Low Noise Current Sink.

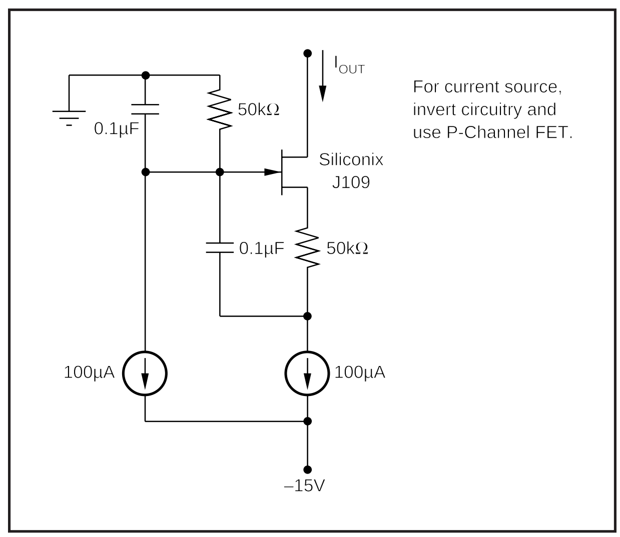


FIGURE 15. Low Noise Current Sink with Compliance Below Ground.

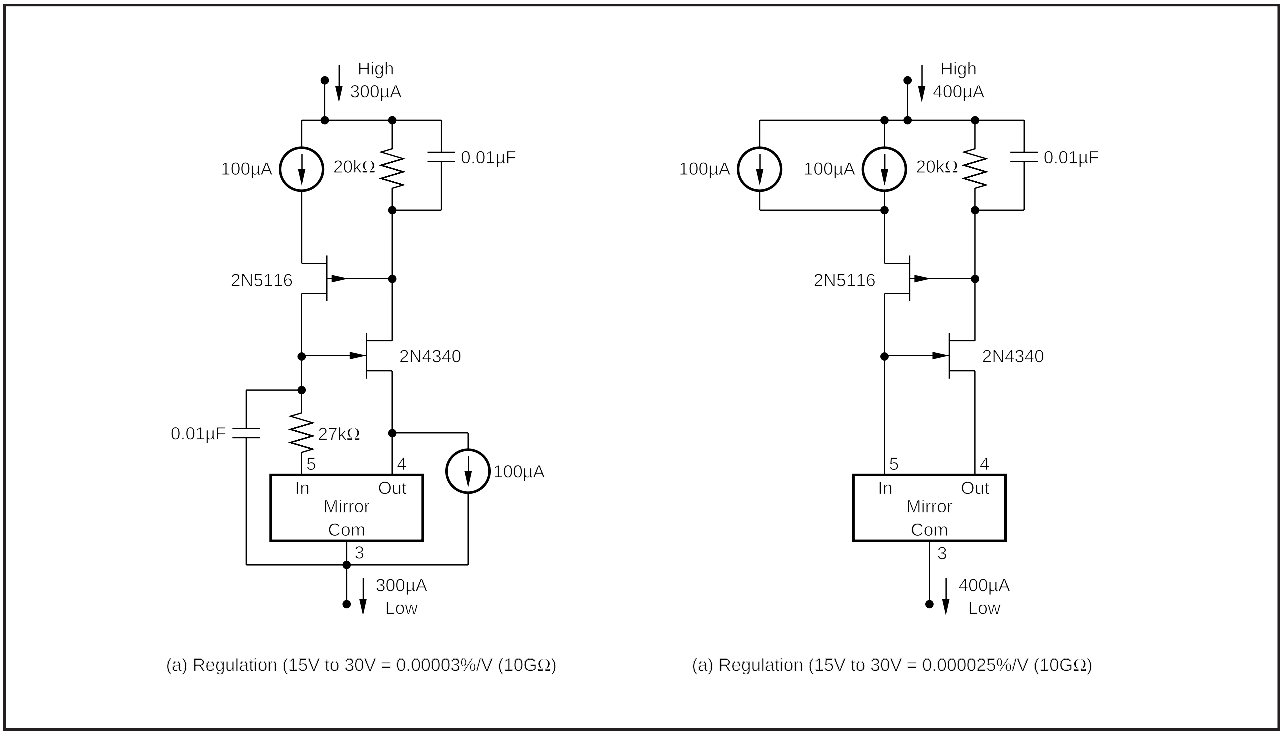


FIGURE 16. Floating 300µA and 400µA Cascoded Current Sources.

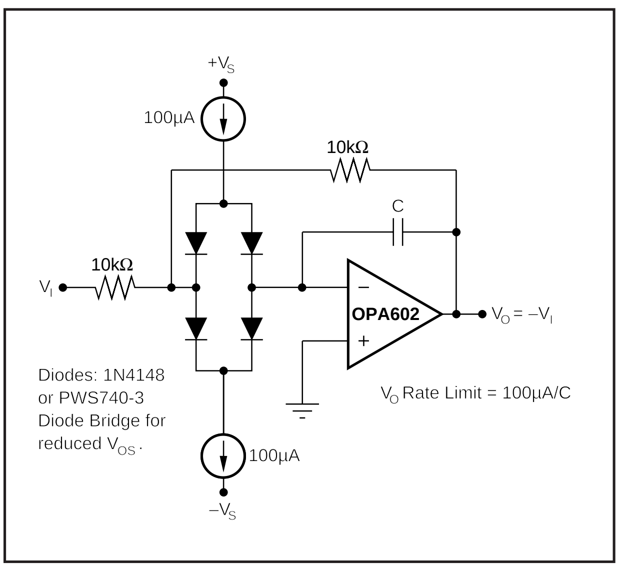


FIGURE 17. Rate Limiter.

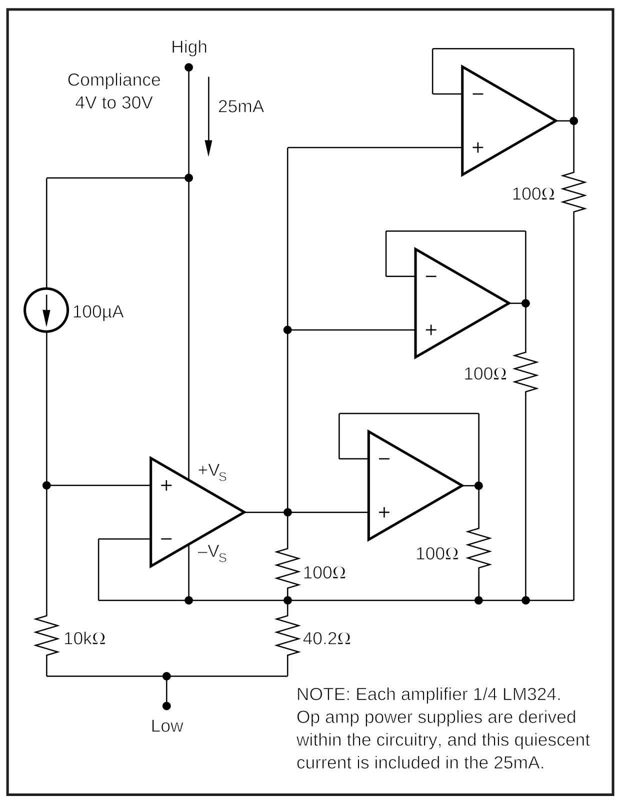


FIGURE 18. 25mA Floating Current Source.

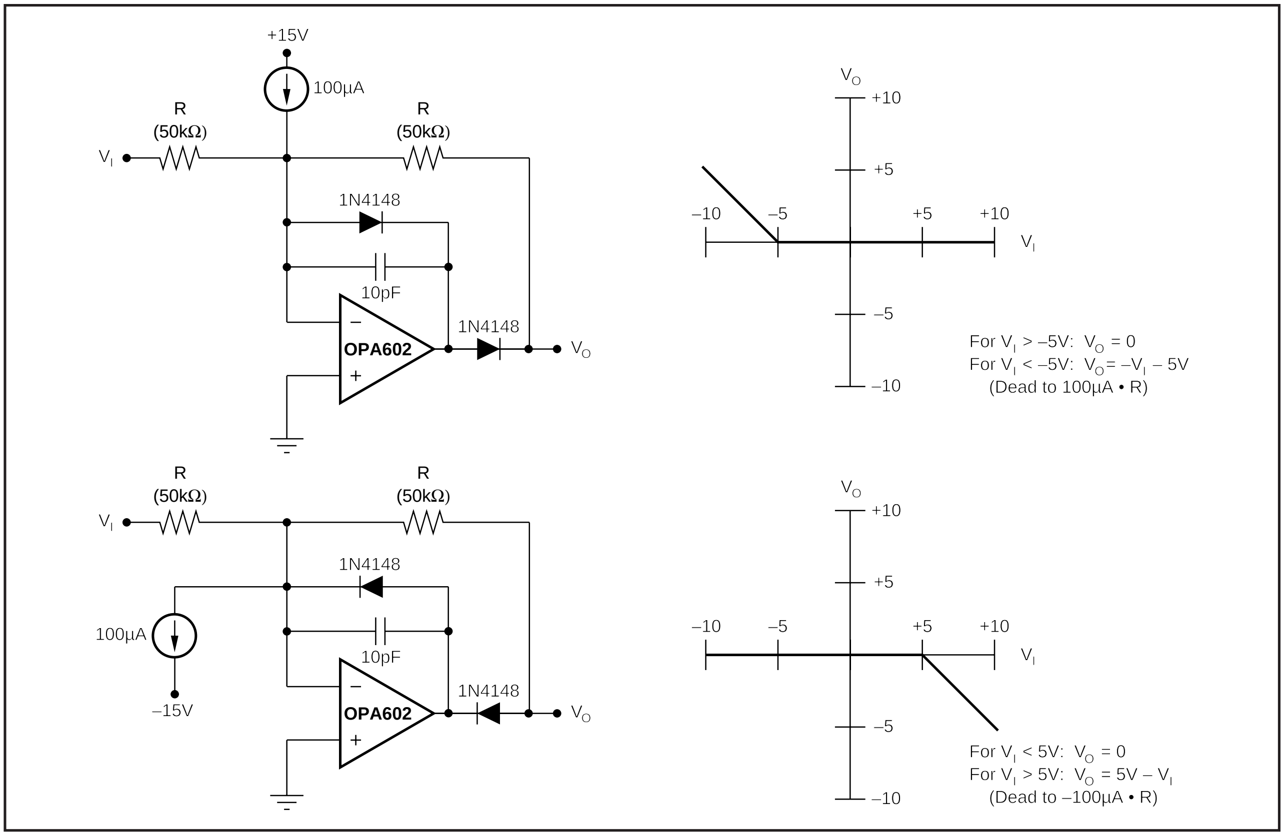


FIGURE 19. Dead-Band Circuit.

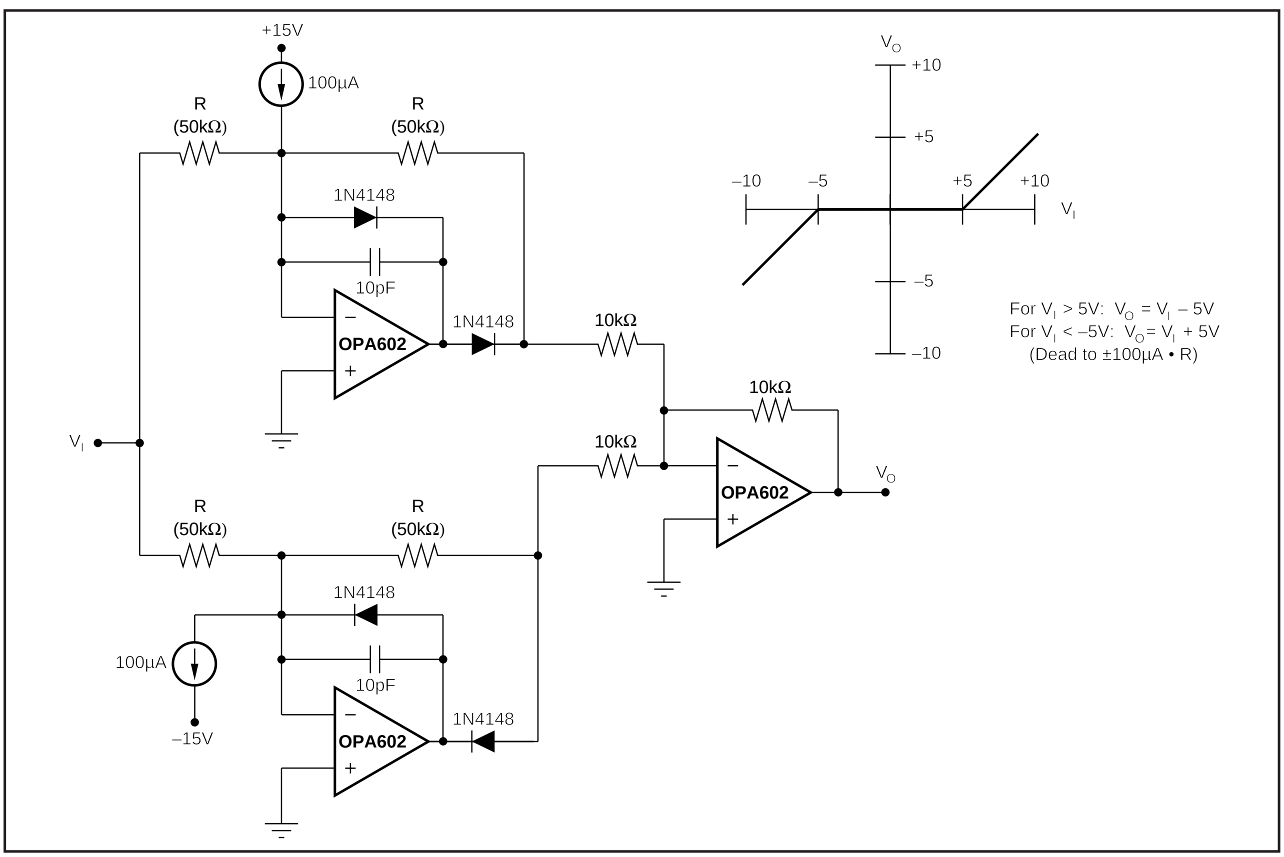


FIGURE 20. Double Dead-Band Circuit.

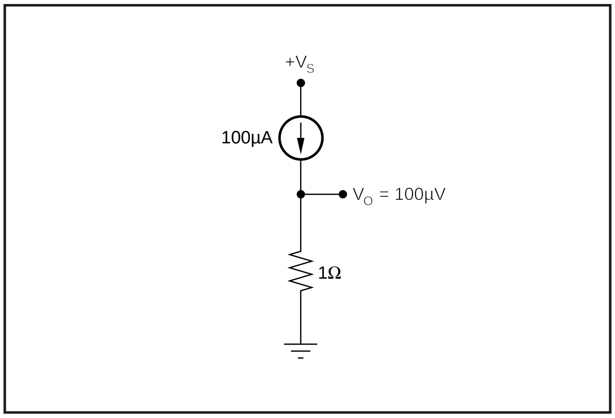


FIGURE 21. Low-Voltage Reference.

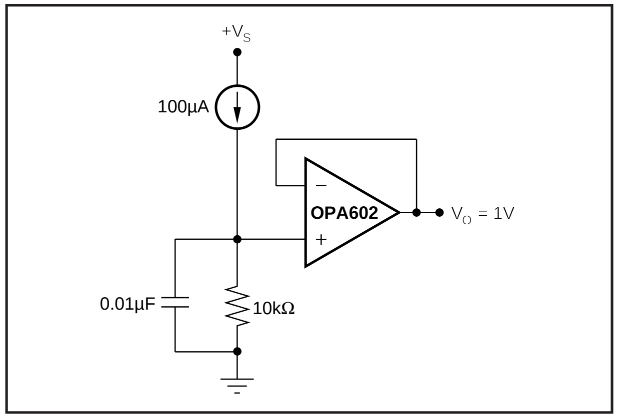


FIGURE 22. Voltage Reference.

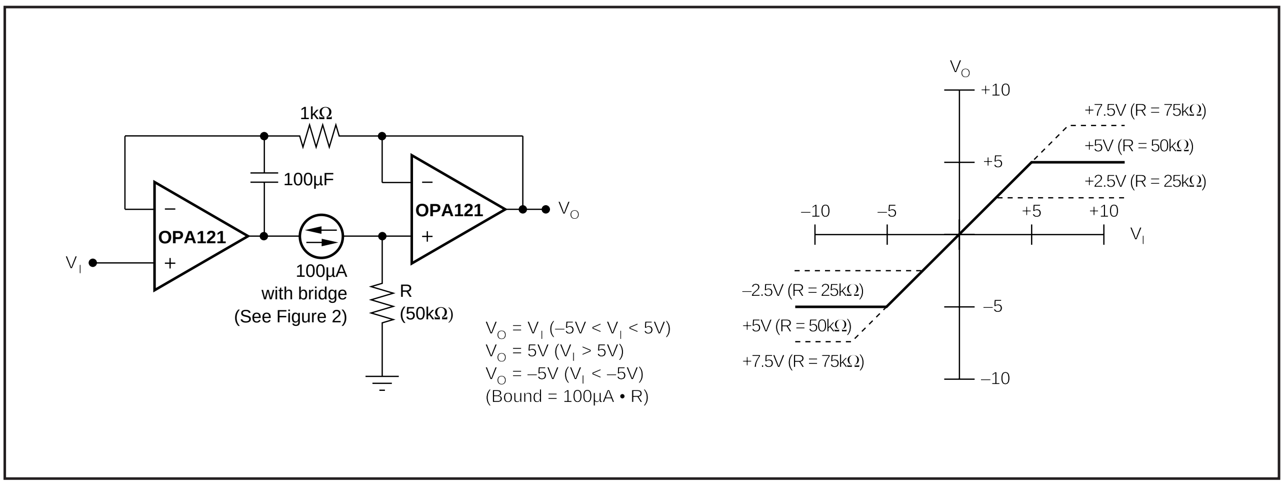


FIGURE 23. Bipolar Limiting Circuit.

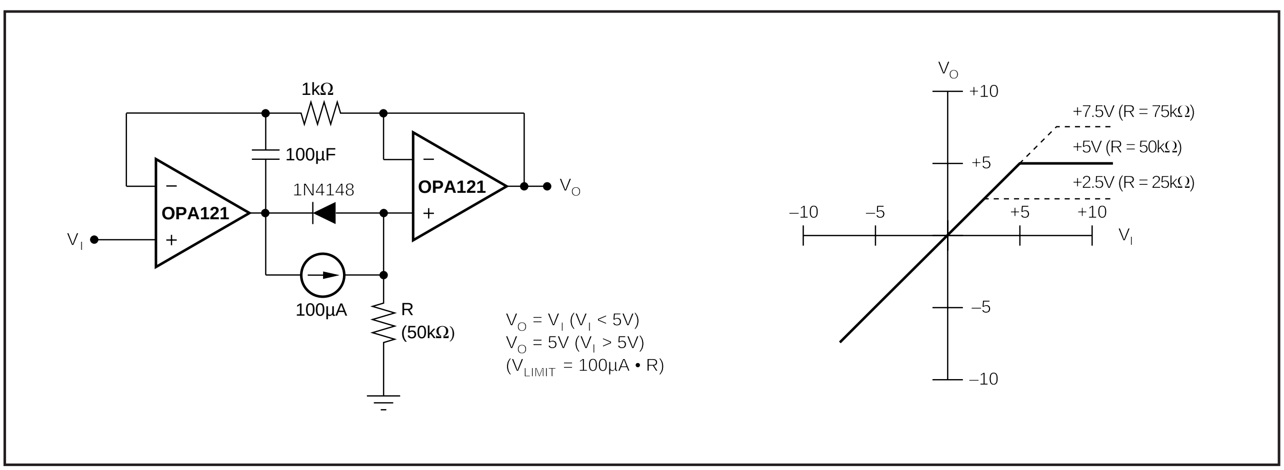


FIGURE 24. Limiting Circuit.

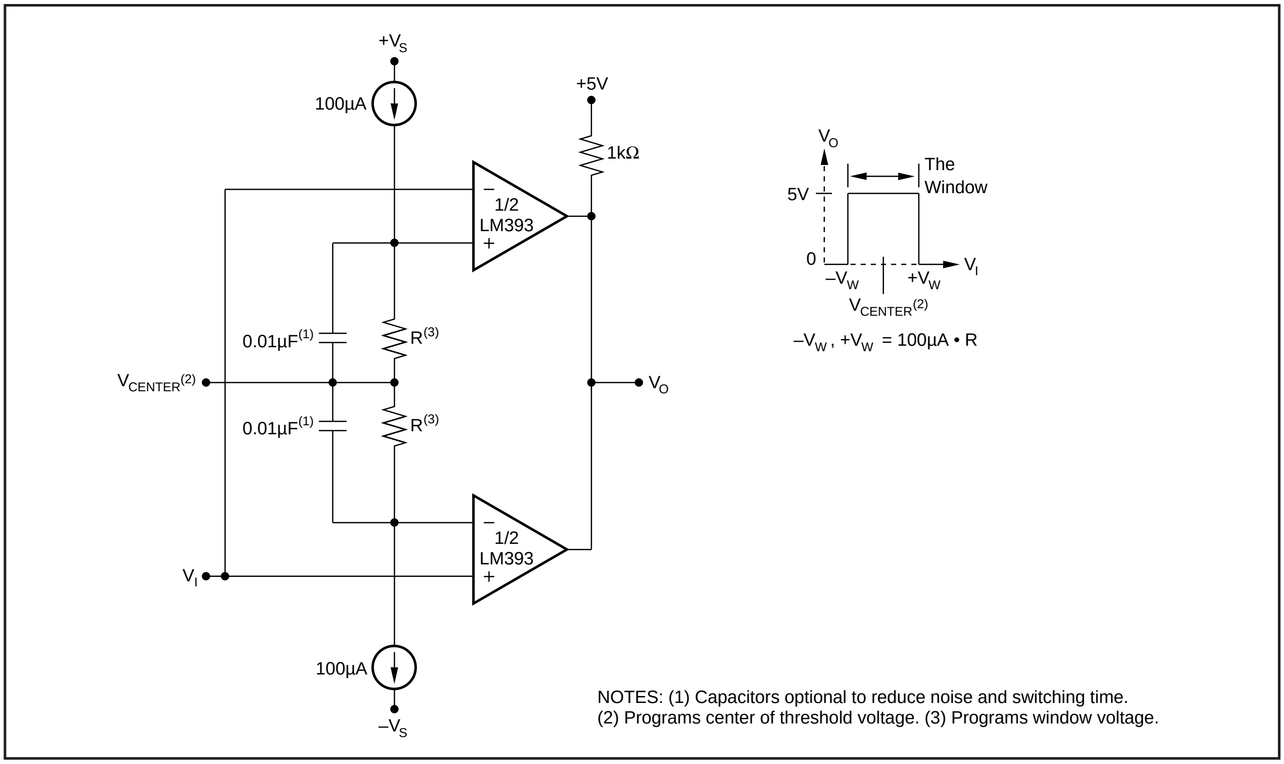


FIGURE 25. Window Comparator.

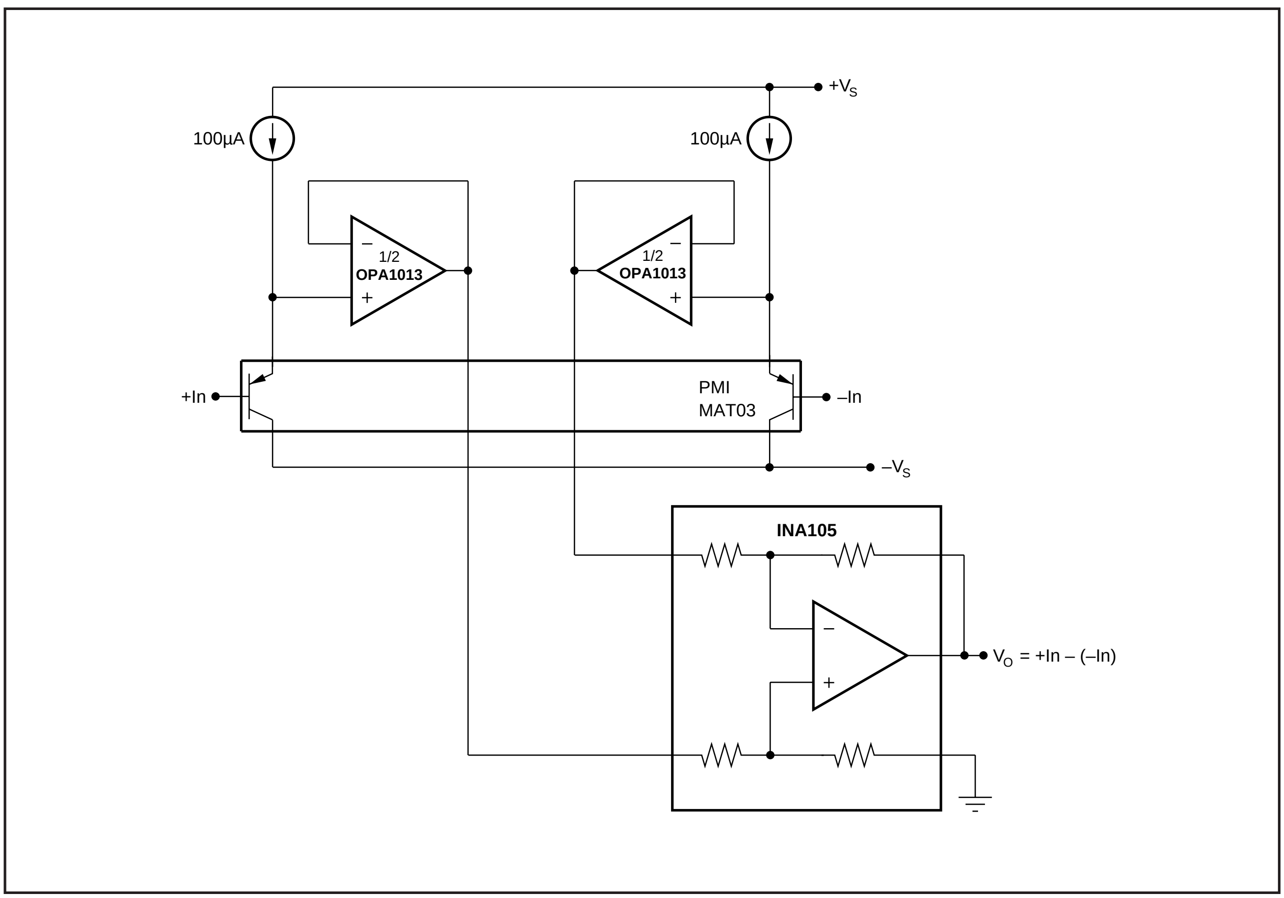


FIGURE 26. Instrumentation Amplifier with Compliance to $-V_S$.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
REF200AP	OBSOLETE	PDIP	P	8		None	Call TI	Call TI
REF200AU	ACTIVE	SOIC	D	8	100	None	CU SNPB	Level-2-220C-1 YEAR
REF200AU/2K5	ACTIVE	SOIC	D	8	2500	None	CU SNPB	Level-2-220C-1 YEAR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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