FEATURES

- COMPLETELY FLOATING: No Power Supply or Ground Connections
- HIGH ACCURACY: 100µA ±0.5%
- LOW TEMPERATURE COEFFICIENT: ±25ppm/°C
- WIDE VOLTAGE COMPLIANCE: 2.5V to 40V
- ALSO INCLUDES CURRENT MIRROR

APPLICATIONS

- SENSOR EXCITATION
- BIASING CIRCUITRY
- OFFSETTING CURRENT LOOPS
- LOW VOLTAGE REFERENCES
- CHARGE-PUMP CIRCUITRY
- HYBRID MICROCIRCUITS

DESCRIPTION

The REF200 combines three circuit building-blocks on a single monolithic chip—two 100µA current sources and a current mirror. The sections are dielectrically isolated, making them completely independent. Also, since the current sources are two-terminal devices, they can be used equally well as current sinks. The performance of each section is individually measured and laser-trimmed to achieve high accuracy at low cost.

The sections can be pin-strapped for currents of 50µA, 100µA, 200µA, 300µA or 400µA. External circuitry can be used to obtain virtually any current. These and many other circuit techniques are shown in the Applications section of this Data Sheet.

The REF200 is available in plastic 8-pin mini-DIP and SOIC packages.
SPECIFICATIONS

ELECTRICAL

At \( T_A = +25^\circ C \), \( V_S = 15V \), unless otherwise noted.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITION</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
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<tbody>
<tr>
<td>CURRENT SOURCES</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current Accuracy</td>
<td>Specified Temp Range</td>
<td>±0.25</td>
<td>±1</td>
<td>%</td>
<td></td>
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<tr>
<td>Current Match</td>
<td></td>
<td>±0.25</td>
<td>±1</td>
<td>%</td>
<td></td>
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<tr>
<td>Temperature Drift</td>
<td></td>
<td></td>
<td>25</td>
<td>ppm/°C</td>
<td></td>
</tr>
<tr>
<td>Output Impedance</td>
<td>2.5V to 40V</td>
<td>20</td>
<td>100</td>
<td>MΩ</td>
<td></td>
</tr>
<tr>
<td></td>
<td>3.5V to 30V</td>
<td>200</td>
<td>500</td>
<td>MΩ</td>
<td></td>
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<tr>
<td>Noise</td>
<td></td>
<td></td>
<td>1</td>
<td>nA/√Hz</td>
<td></td>
</tr>
<tr>
<td>( f = 10kHz )</td>
<td></td>
<td></td>
<td>20</td>
<td>pA/√Hz</td>
<td></td>
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<tr>
<td>Voltage Compliance (1%)</td>
<td></td>
<td></td>
<td>See Curves</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Capacitance</td>
<td></td>
<td></td>
<td>10</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>CURRENT MIRROR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I = 100µA )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gain</td>
<td></td>
<td>0.995</td>
<td>1</td>
<td>1.005</td>
<td></td>
</tr>
<tr>
<td>Temperature Drift</td>
<td></td>
<td></td>
<td>25</td>
<td>ppm/°C</td>
<td></td>
</tr>
<tr>
<td>Impedance (output)</td>
<td>2V to 40V</td>
<td>40</td>
<td>100</td>
<td>MΩ</td>
<td></td>
</tr>
<tr>
<td>Nonlinearity</td>
<td></td>
<td></td>
<td>0.05</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>Input Voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Compliance Voltage</td>
<td>I = 0µA to 250µA</td>
<td></td>
<td>1.4</td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td>See Curves</td>
<td></td>
<td></td>
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<tr>
<td>Frequency Response (~3dB)</td>
<td></td>
<td></td>
<td>5</td>
<td>MHz</td>
<td></td>
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<tr>
<td>TEMPERATURE RANGE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Specification</td>
<td></td>
<td>−25</td>
<td>+85</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Operating</td>
<td></td>
<td>−40</td>
<td>+85</td>
<td>°C</td>
<td></td>
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<tr>
<td>Storage</td>
<td></td>
<td>−40</td>
<td>+125</td>
<td>°C</td>
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PIN CONFIGURATION

Top View

DIP/SOIC

<table>
<thead>
<tr>
<th>I1 Low</th>
<th>I1 High</th>
<th>I2 Low</th>
<th>I2 High</th>
<th>Mirror Common</th>
<th>Mirror Output</th>
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</thead>
<tbody>
<tr>
<td>1</td>
<td>8</td>
<td>2</td>
<td>7</td>
<td>3</td>
<td>6</td>
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</table>

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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TYPICAL PERFORMANCE CURVES

At \( T_A = +25^\circ C \), \( V_S = +15V \), unless otherwise noted.

1. **CURRENT SOURCE TYPICAL DRIFT vs TEMPERATURE**
   - Drift specified by "box method" (See text)
   - Drift at 85°C

2. **CURRENT SOURCE TEMPERATURE DRIFT DISTRIBUTION**
   - Distribution of three production lots — 1284 Current Sources.
   - Quantity (Units)

3. **CURRENT SOURCE OUTPUT CURRENT vs VOLTAGE**
   - Output Current (µA)

4. **CURRENT SOURCE CURRENT NOISE (0.1Hz to 10Hz)**
   - Time (500ms/div)

5. **CURRENT SOURCE REVERSE CURRENT vs REVERSE VOLTAGE**
   - Safe Reverse Current
   - Safe Reverse Voltage
   - Reverse Voltage Circuit Model
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ C$, $V_S = +15V$, unless otherwise noted.

- **MIRROR GAIN ERROR vs CURRENT**
- **MIRROR TRANSFER NONLINEARITY**
- **MIRROR INPUT VOTAGE/OUTPUT COMPLIANCE VOLTAGE vs CURRENT**
APPLICATIONS INFORMATION

The three circuit sections of the REF200 are electrically isolated from one another using a dielectrically isolated fabrication process. A substrate connection is provided (pin 6), which is isolated from all circuitry. This pin should be connected to a defined circuit potential to assure rated DC performance. The preferred connection is to the most negative constant potential in your system. In most analog systems this would be −V_S. For best AC performance, leave pin 6 open and leave unused sections unconnected.

Drift performance is specified by the “box method,” as illustrated in the Current vs Temperature plot of the typical performance curves. The upper and lower current extremes measured over temperature define the top and bottom of the box. The sides are determined by the specified temperature range of the device. The drift of the unit is the slope of the diagonal—typically 25ppm/°C from −25°C to +85°C.

If the current sources are subjected to reverse voltage, a protection diode may be required. A reverse voltage circuit model of the REF200 is shown in the Reverse Current vs Reverse Voltage curve. If reverse voltage is limited to less than 6V or reverse current is limited to less than 350µA, no protection circuitry is required. A parallel diode (Figure 2a) will protect the device by limiting the reverse voltage across the current source to approximately 0.7V. In some applications, a series diode may be preferable (Figure 2b) because it allows no reverse current. This will, however, reduce the compliance voltage range by one diode drop.

Applications for the REF200 are limitless. Application Bulletin AB-165 shows additional REF200 circuits as well as other related current source techniques. A collection of circuits is shown to illustrate some techniques. Also, see AB-165A.
FIGURE 3. 50µA Current Source.

FIGURE 4. 200µA, 300µA, and 400µA Floating Current Sources.

FIGURE 5. 50µA Current Sinks.
FIGURE 6. Improved Low-Voltage Compliance.

FIGURE 7. 100µA Current Source—80V Compliance.

FIGURE 8. FET Cascode Circuits.

NOTES: (1) FET cascoded current sources offer improved output impedance and high frequency operation. Circuit in (b) also provides improved PSRR. (2) For current sinks (Circuits (a) and (b) only), invert circuits and use "N" channel JFETS.

Using Standard Potentiometer

\[
V_{\text{OUT}} = V_{\text{IN}} \left( -\frac{R_2}{R_3} \right)
\]
Offset Adjustment Range = ±5mV

NOTE: (1) For N Op Amps, use Potentiometer Resistance = N × 100Ω.

Using Bourns Op Amp Trimpot

\[
V_{\text{OUT}} = -V_{\text{IN}} \left( \frac{R_2}{R_3} \right)
\]
Offset Adjustment Range = ±5mV

(1) Bourns Trimpot

Linear
EXAMPLES

**FEATURES:**
(1) Zero volts shunt compliance.
(2) Adjustable only to values above reference value.

**NOTE:**
Current source/sink swing to the "Load Return" rail is limited only by the op amp's input common mode range and output swing capability. Voltage drop across "R" can be tailored for any amplifier to allow swing to zero volts from rail.

<table>
<thead>
<tr>
<th>R</th>
<th>NR</th>
<th>I_{out}</th>
</tr>
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<tbody>
<tr>
<td>1kΩ</td>
<td>4kΩ</td>
<td>500µA</td>
</tr>
<tr>
<td>1kΩ</td>
<td>9kΩ</td>
<td>1mA</td>
</tr>
<tr>
<td>10kΩ</td>
<td>9.9kΩ</td>
<td>10mA</td>
</tr>
</tbody>
</table>

**EXAMPLES**

I_{out} = N \cdot 100µA

**FIGURE 10.** Adjustable Current Sources.
FIGURE 11. RTD Excitation With Three Wire Lead Resistance Compensation.

FIGURE 12. Precision Triangle Waveform Generator.
FIGURE 13. Precision Duty-Cycle Modulator.

For current source, invert circuitry and use P-Channel FET.

FIGURE 14. Low Noise Current Sink.

FIGURE 15. Low Noise Current Sink with Compliance Below Ground.
FIGURE 16. Floating 300\mu A and 400\mu A Cascoded Current Sources.

FIGURE 17. Rate Limiter.

FIGURE 18. 25mA Floating Current Source.
For $V_i > -5V$: $V_O = 0$  
For $V_i < -5V$: $V_O = -V_i - 5V$  
(Dead to $100\mu A \cdot R$)

For $V_i < 5V$: $V_O = 0$  
For $V_i > 5V$: $V_O = 5V - V_i$  
(Dead to $-100\mu A \cdot R$)

FIGURE 19. Dead-Band Circuit.

For $V_i > -5V$: $V_O = 0$  
For $V_i < -5V$: $V_O = -V_i - 5V$  
(Dead to $100\mu A \cdot R$)

For $V_i < 5V$: $V_O = 0$  
For $V_i > 5V$: $V_O = 5V - V_i$  
(Dead to $-100\mu A \cdot R$)

FIGURE 20. Double Dead-Band Circuit.

FIGURE 22. Voltage Reference.

FIGURE 23. Bipolar Limiting Circuit.

FIGURE 24. Limiting Circuit.
FIGURE 25. Window Comparator.

FIGURE 26. Instrumentation Amplifier with Compliance to $-V_S$.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp (3)</th>
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<td>REF200AP</td>
<td>OBSOLETE</td>
<td>PDIP</td>
<td>P</td>
<td>8</td>
<td>None</td>
<td>Call TI</td>
<td>Call TI</td>
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<tr>
<td>REF200AU</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>100</td>
<td>CU SNPB</td>
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<td>REF200AU/2K5</td>
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<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>CU SNPB</td>
<td>Level-2-220C-1 YEAR</td>
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(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

** OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - May not be currently available - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.

**None:** Not yet available Lead (Pb-Free).

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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<th>Applications</th>
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<tbody>
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<td>Amplifiers</td>
<td>Audio</td>
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<td>Data Converters</td>
<td>Automotive</td>
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